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LOW TEMPERATURE MATERIALS GROWTH AND PROCESSING DEVELOPMENT FOR FLAT PANEL DISPLAY TECHNOLOGY APPLICATIONS

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Subj: RETURNED GRANTEE/CONTRACTOR TECHNICAL REPORTS

1. This confirms our conversations of 27 Feb 97 and 11 Jul 97. Enclosed are a number of technical reports which were returned to our agency for lack of clear distribution availability statement. This confirms that all reports are unclassified and are "APPROVED FOR PUBLIC RELEASE" with no restrictions.

2. Please contact me if you require additional information. My e-mail is *silverr@onr.navy.mil* and my phone is (206) 625-3196.

ROBERT J. SILVERMAN

FIELD EMITTER FLAT PANEL RESULTS

Anthony E Bell, Associate Professor

Graduate Assistants: Kit-sing Mak and Haibing Liu

Objectives:

a) To understand the relative advantages and properties of diamond and graphite nanotubes as emission sources for FED displays.

b) To develop methods of growing uniform deposits of graphite (fullerene) nanotubes of nanometer scale diameters. It is believed that these field emitters will have the following properties:

1. Low turn-on voltages
2. Insensitivity to the vacuum ambient.
3. Inexpensive methods of preparation
4. A compatibility with other industrial efforts,e.g., that of S.I. Diamond Corp.

c) To develop focused electron beam and focused ion beam (FIB) techniques for repairing flat panel display panels, especially those utilizing active matrix technology involving relatively small line widths.

Method of Approach:

a) Measure the work function, using a geometry independent absolute method, of diamond, both doped and undoped diamond, in order to establish the claims of ultra-low work function of n-doped diamond substrates.

b) Grow graphite nanotubes on Fe nuclei seeded on Si wafers and characterize them by inserting them in a vacuum viewing apparatus with a phosphor screen in order to ascertain the uniformity of electron emission over an area 1 cm x 1 cm. The wafer is heavily doped in order to be electrically conductive and is miscut by 5 degrees so that there will be a uniform density of step edge defects capable of accommodating and attracting the vacuum deposited Fe nanometer scale nuclei on which to anchor the growing carbon nanotubes.

c) Study different methods of depositing nanotubes, including plasma techniques.

d) Investigate methods of depositing metals and insulators using either electron and ion beams. Do this in collaboration with FEI Corporation, a local manufacturer of FIB and electron focused elctron beam systems.

Results:

a) Work has been devoted towards processing silicon wafers to provide a support structure with a 1 cm x 1 cm x 2 micron deep recess for depositing the graphite nanotubes. A supported tungsten mesh will be used as an anode. This structure will enable reliable measurements to be made of the nanotube uniformity for electron emission. Good results have been obtained for yields of nanotubes using a toluene/hydrogen feed for the CVD deposition process used.

Kit-Sing Mak has developed 2 and 3 dimensional models for temperature induced effects due to ion and electron beam bombardment in solids of different thermal conductivities. Some experimental work has also been accomplished using electron high current density electron beam heating of SiO_2. A field emitter electron source was used in a high performance SEM at FEI Corp. of Hillsboro, Oregon.

Work for the next quarter:

a) Work will commence in using the FEI equipment to investigate advanced methods for depositing insulators and metals using focused electron beams.

b) Work will be devoted to completing development of the silicon support structure and to viewing the uniformity of the electron emission on a phosphor screen.

Modeling of a-Si TFTs for Liquid Crystal Display Applications

V. S. Rao Gudimetla

Department of Electrical Engineering and Applied Physics
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Background:

The project goal is to make DC, AC, transient measurements on the TFTs, fabricated by Professor Sigmon and his group at Lawrence Livermore National Laboratory using low temperature processing techniques. From these measurements, SPICE parameters will be extracted and these results will be used for process monitoring and device and process optimization for display applications. This work was started by Rao Gudimetla on 10/1/94 and this technical report is for the period 11/15/95 to 2/14/96.

Work Schedule and Results:

During the above project period, Rao Gudimetla spent part of his time teaching two courses and remainder of the time at Lawrence Livermore National Laboratory (LLNL) as a Participating Guest.

As given in my previous report, several of the TFTs have poor drain to source current (Ids) and high threshold voltages. Extensive simulations have indicated some possible sources of errors in the fabrication. No new devices that have significant overlap between source/gate contacts and drain/gate contacts were yet fabricated to eliminate its role if any. Similarly plans are under way to hydrogenate the devices to check if a-Si is very defective which might have been the reason for high threshold voltages. We started to develop Spice models although the devices are not good and the data is unstable and AIM Spice modeling is being pursued. Initial analysis of several devices indicate that the contact resistances are high. In the absence of capacitance data, no definitive conclusion was reached with regard to the role of defect states. We have plans to collect capacitance data on well behaving devices.

We will analyze several more devices to get the SPICE models and extract device parameters to check the accuracy of device fabrication.

Immediate Future Goals:

We will wait for the devices to be fabricated and test those devices for AC and capacitance data. With recent hiring of two process engineers at LLNL, I expect that the devices would be delivered soon. Meanwhile, we continue to build Spice models for the existing devices, including grain boundary and mobility models. Also couple of papers, based on the work so far, will be submitted this quarter. These include AC modeling of TFTs and critical review of defect state effects on TFT electrical characteristics.

I. SUMMARY

The primary purpose of this research effort is to investigate and characterize the use of Gas Immersion Laser Doping (GILD) for the fabrication of polysilicon thin-film transistors (TFTs). GILD is used in two process steps in the fabrication of poly-Si TFTs, being the laser recrystallization of the channel region, and the doping of the source and drain regions. We are currently optimizing the laser conditions for the former process step, and will optimize the latter step in the future. The last report discussed the results of TEM studies on unpatterned poly-Si films on an oxidized silicon wafer, irradiated at many different laser energies. This report presents results from a TEM study on prepatterned poly-Si films on oxidized wafers, which were subjected to the same irradiation conditions as the previous unpatterned poly-Si films. The resulting grain microstructure from the irradiated prepatterned films are compared with those obtained using unpatterned films. It is important to identify the difference in final microstructure provided by these two systems since this study has not been done yet, and researchers currently pick a system randomly, assuming that there is no difference.

II. TECHNICAL DISCUSSION

This experiment was performed exactly as the unpatterned poly-Si film experiment detailed in the last report, except that the 100 nm poly-Si film on the oxidized silicon wafer was patterned into islands before laser recrystallization. The island patterns consisted of squares of length, and circles of diameter, 4, 10, 14, 20, 24, 30, 36, 40, 50, and 60 microns. Irradiation used ten laser pulses from a XeCl excimer laser operating at 308 nm. Irradiation energies ranged from surface heating to ablation.

In all cases, the grain structure inside the island was always the same as that in the unpatterned case seen in the last section. However, large elongated grains grew along the edge of each island for an energy range beginning at the full-melt threshold energy, as shown in Figure 1. The reason for these large grains is derived from a two-dimensional cooling effect that occurs only along the edge of the island. As illustrated in Figure 2, when an island is completely molten, the center cools by transferring its heat down into the substrate. Nucleation occurs at the poly-Si / oxide interface as in the unpatterned case, and fine grain growth results. The edge of the island transfers its heat down into the substrate, *and* outward in the substrate in the plane of the island. Since the edge has an additional dimension to cool into the substrate, the edge cools before the center and a temperature gradient is set up. This temperature gradient causes the grains to nucleate first at the edge of the island, which is cooled first. Then this gradient pushes the melt front towards the center of the island, creating elongated grains. These elongated grains stop growing when the temperature gradient disappears, at which time the center part of the island cools and nucleates fine grains. In summary, prepatterning the poly-Si into islands creates a temperature gradient along their edges that causes grain nucleation at the edge and propagates the melt front inwards for the duration that the temperature gradient exists, after which the rest of the island nucleates

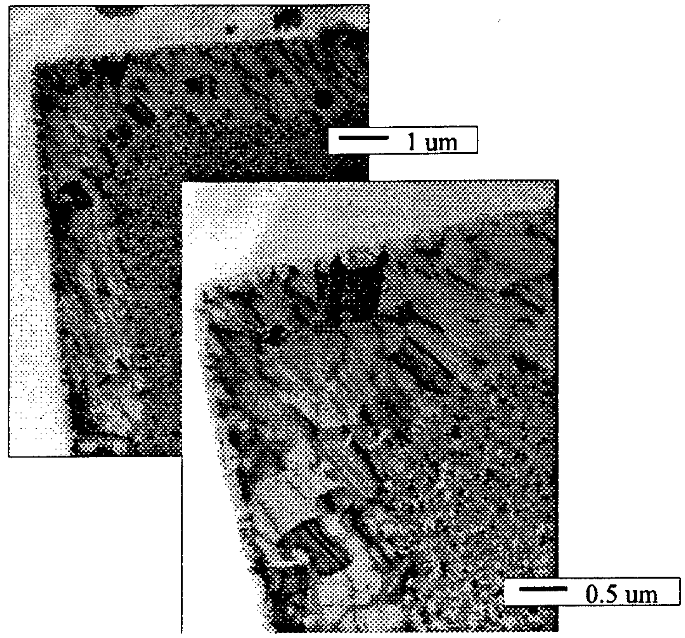

Figure 1 TEM plan-view photos showing 2-D cooling effect from prepatterned poly-Si films during laser recrystallization.

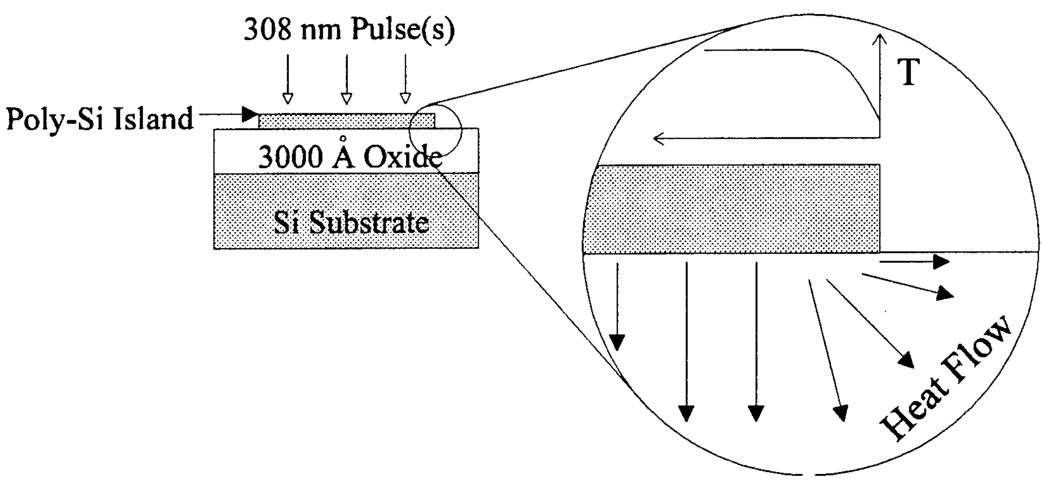

Figure 2 Illustration of 2-D cooling effect during laser recrystallization of a prepatterned poly-Si island. The edge cools first, setting up a temperature gradient. The grains nucleate at the edge and the temperature gradient drives the melt front inwards.

off of the poly-Si / oxide interface and resolidifies simultaneously into fine grains.

Prepatterning the poly-Si film before laser recrystallization is therefore one method of grain engineering that controls the heat flow to produce large grains in a lithographically determined location. The grain structure along the edge of each island was uneffected by the island length or diameter. However, if the island size was made small enough, the temperature gradient extended over the entire island, producing large grains everywhere. The left of Figure 3 shows a 4 um square island consisting entirely of large grains. Note that the laser processed island is somewhat smaller than 4 um, as surface tension when molten causes the island to shrink. Atomic force microscopy indicates that the large-grained regions are thicker than the fine-grained regions. At higher laser energies, only the corners contained large grains, as shown in the right of Figure 3. Here, three-dimensional cooling occurs; the corner cools by transferring heat down into the substrate, and radially away from the corner in the plane of the island.

Such enlargement of grains along the edges and corners was seen over an appreciable energy range. Higher incident laser energies produced fine grain poly-Si everywhere in the island. Still higher energies ablated the islands. This research is important because when researchers laser recrystallize their poly-Si films, it is usually random whether they use unpatterned or prepatterned poly-Si films.

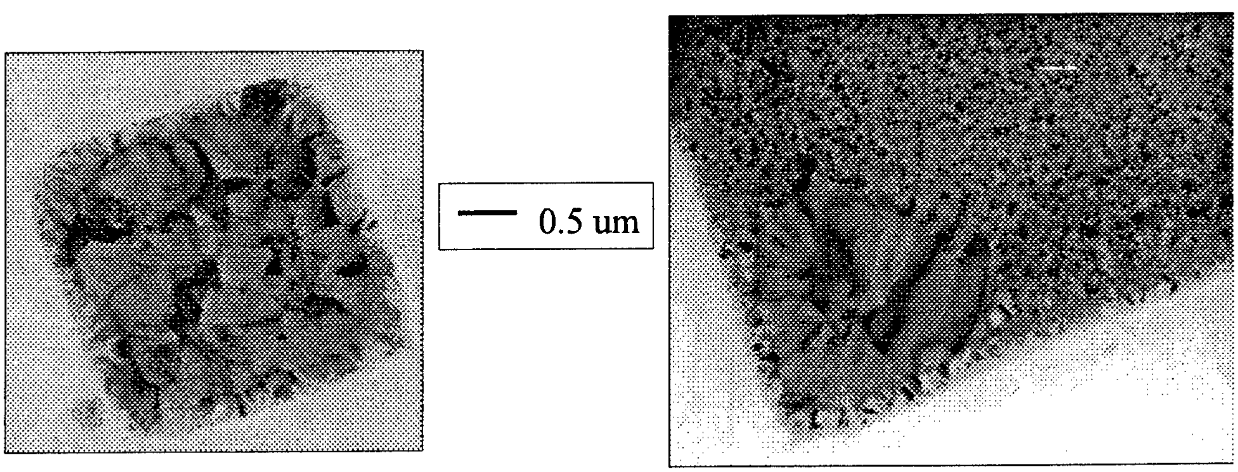

Figure 3 TEM plan-view photos showing (left) small island consisting entirely of large grains resulting from 2-D and/or 3-D cooling effects after laser recrystallization, and (right) 3-D cooling effect seen in corner after laser recrystallization.

IV. FUTURE WORK

Future work will concentrate on the two key areas that GILD will be used in fabricating high performance TFTs. The first application is to recrystallize the channel poly-Si. We will investigate new methods of grain engineering, to increase the final recrystallized grain size and quality. The second GILD application is to dope the source and drain regions. Future efforts will optimize the laser conditions for obtaining low resistivity junctions, while minimizing the number of doping laser pulses. Having these two steps optimized, fully GILD processed TFTs will be fabricated and tested.

<u>Quarterly Report</u>

Electroluminescent Displays Research Group

PIs: R. Engelmann and R. Solanki

Graduate Student: J. Ferguson

Traditional electroluminesent (EL) phosphors consist of wide bandgap semiconductors that are doped with appropriate activators, where the latter are the source of light. We are investigating a new concept for EL phosphors where instead of activators, light is produced from artificially engineered materials, i.e., multiple quantum well (MQW) structures.

We have already demonstrated the proof of concept of MQW EL phosphors in SrS/CdSe system, as described in our last progress report. However, the brightness in this material system was low. We are continuing our investigation to increase the EL brightness and produce the emission at shorter wavelengths. To achieve this objective, we have started to examine CaS/ZnS MQW system. Our progress to date is described below.

The CaS/ZnS MQW system will consist of 40nm thick wide bandgap (4.4eV) CaS, alternated with 50 nm thick narrower bandgap (2.7 eV) ZnSe layers. Initially, we plan to fabricate EL phosphors with 10 QWs.

To achieve this objective, over the past quarter we have been investigating atomic layer epitaxy (ALE) of ZnSe using elemental Zn and Se precursors. This has involved optimization of all the ALE growth parameters: source and substrate temperatures, pulse width of the precursors and nitrogen (which is the purge gas), as well as the nitrogen flows in the inner and outer tubes. The substrates have been plain 2 inch X 2 inch glass plates. This segment of our investigation is now complete. X-ray diffraction pattern of ALE grown ZnSe on a glass substrate is shown in Fig. 1. The three peaks (from largest to smallest) correspond to diffraction from (111), (220) and (222) planes of the cubic phase.

We are now in the process of investigating ALE growth of CaS. The precursors for Ca and S we plan to utilize are Bis (2,2,6,6-tetramethyl-3,5-heptanedionato) calcium and hydrogen sulphide, respectively. Once the ALE parameters for growth of CaS are optimized, then we shall fabricate CaS/ZnSe MQW structures. These results will be described in our next progress report.

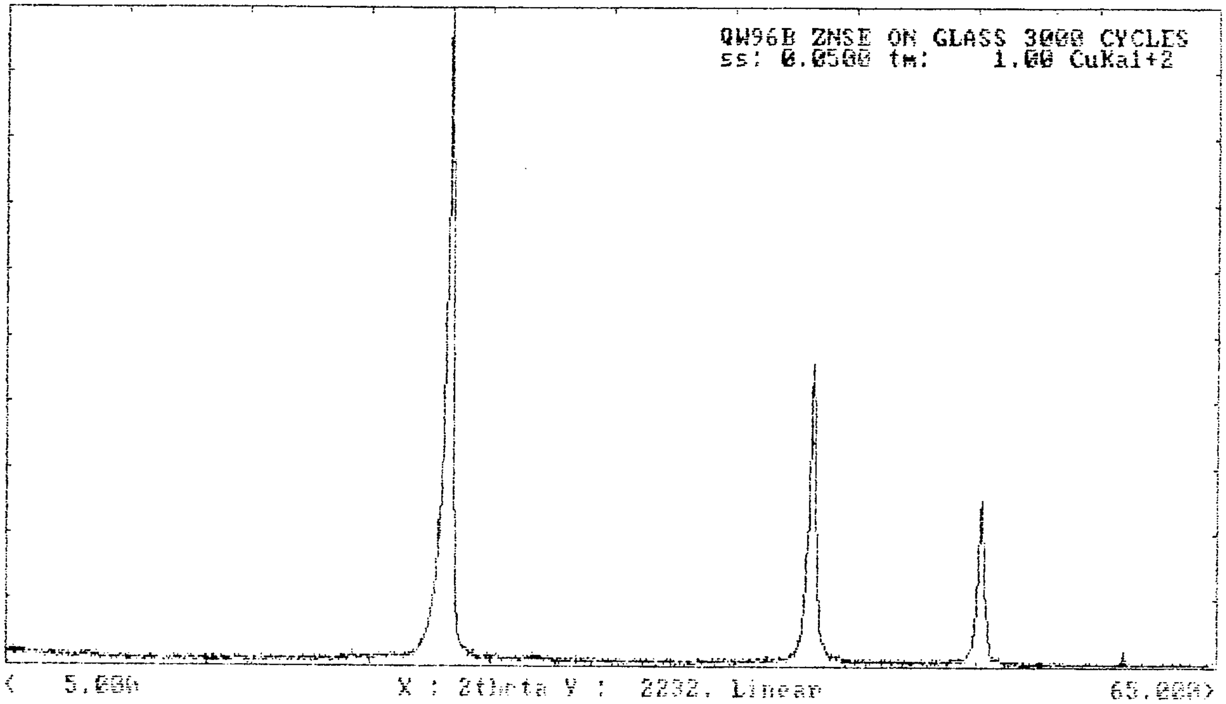

Figure 1. X-ray diffraction spectrum (2Θ) of ALE grown ZnSe.